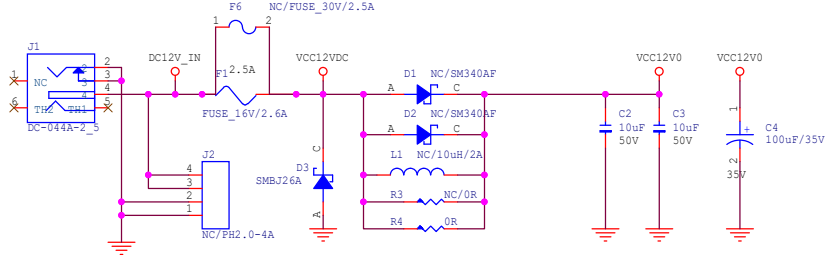
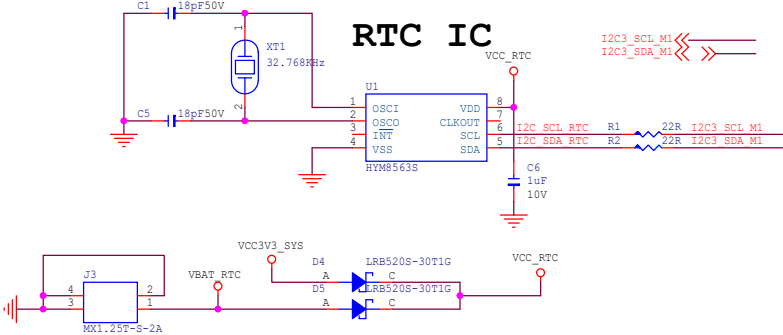




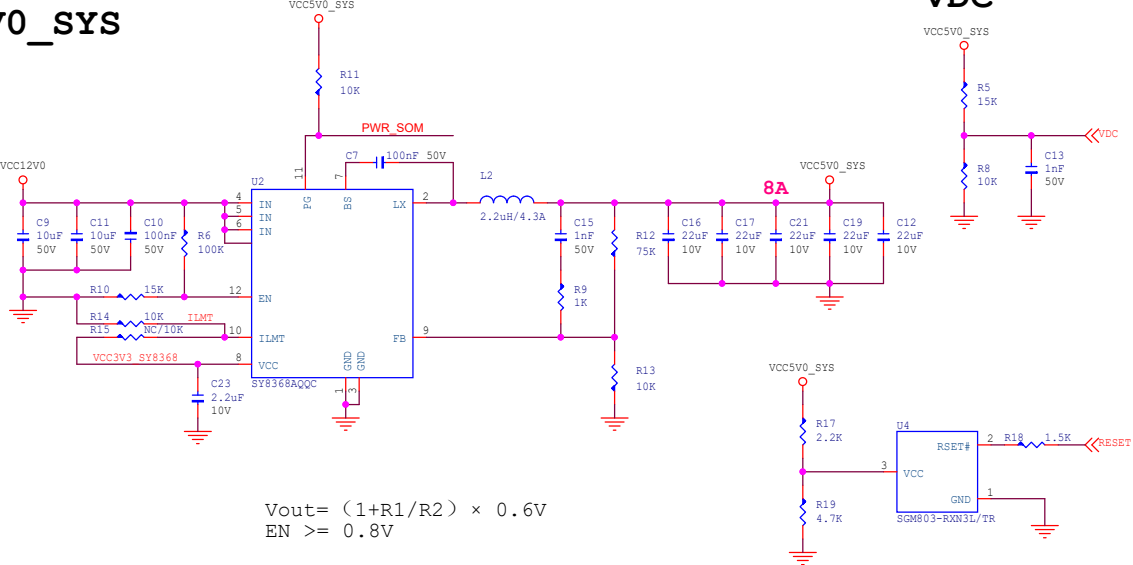
12V/3A DCIN



RTC IC

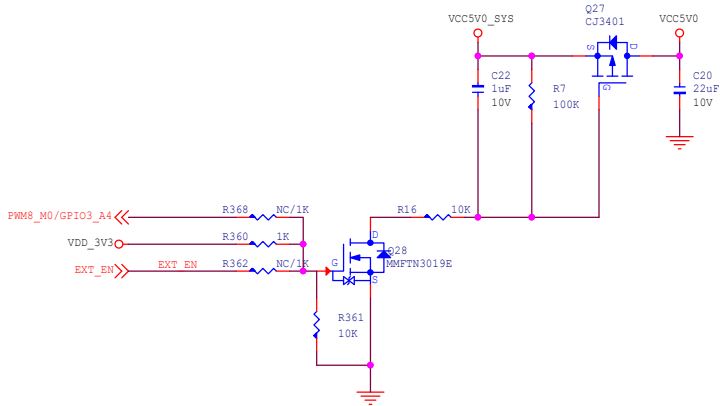


VCC5V0_SYS

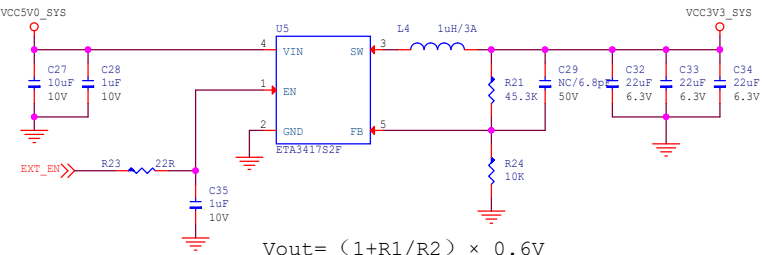


$$V_{out} = (1 + R1/R2) \times 0.6V$$
$$EN \geq 0.8V$$

VCC5V0

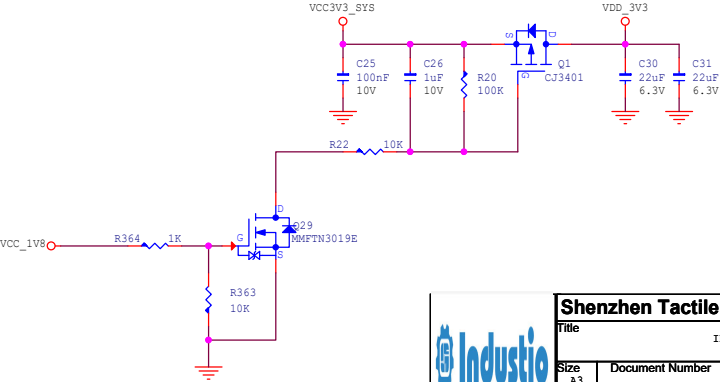


VCC3V3_SYS

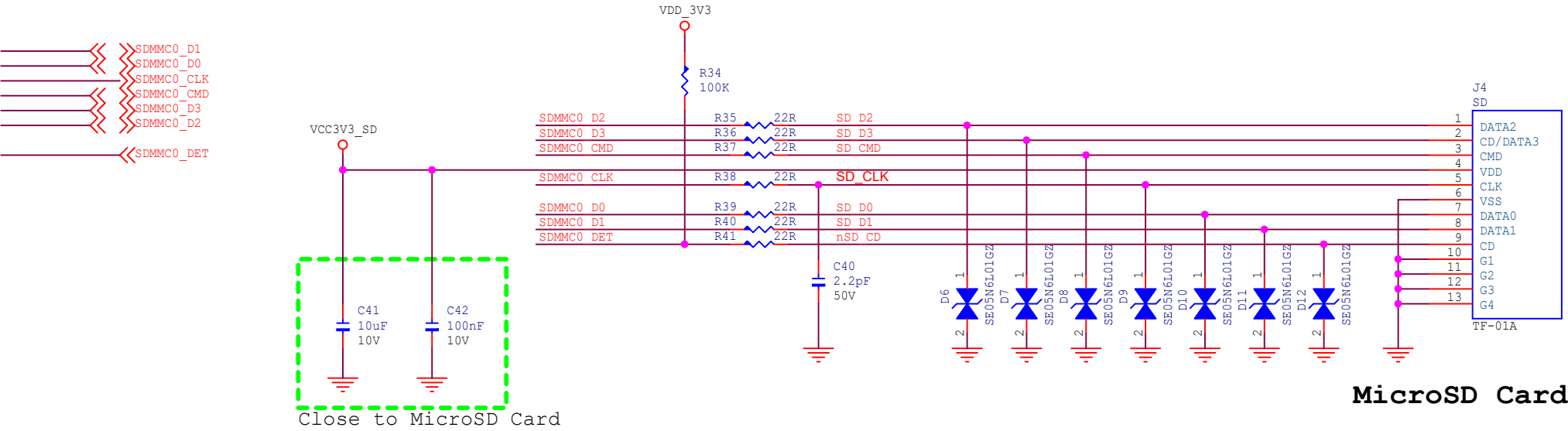


$$V_{out} = (1 + R1/R2) \times 0.6V$$
$$EN \geq 1.5V$$

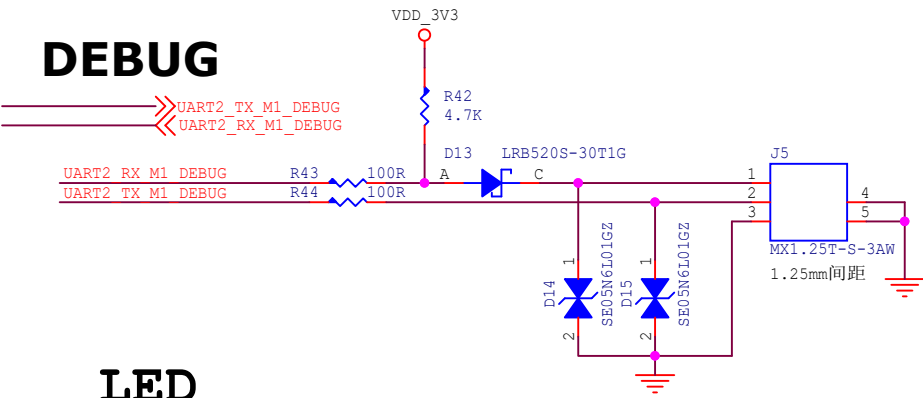
VDD_3V3



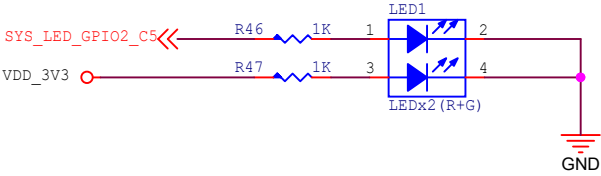
TF CARD



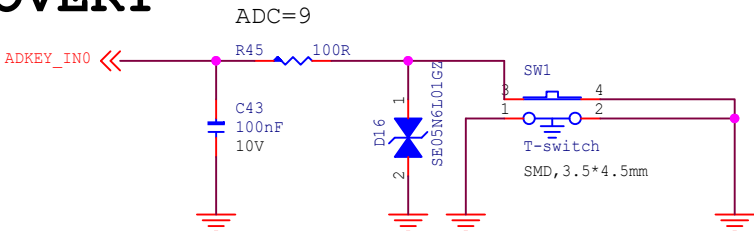
DEBUG



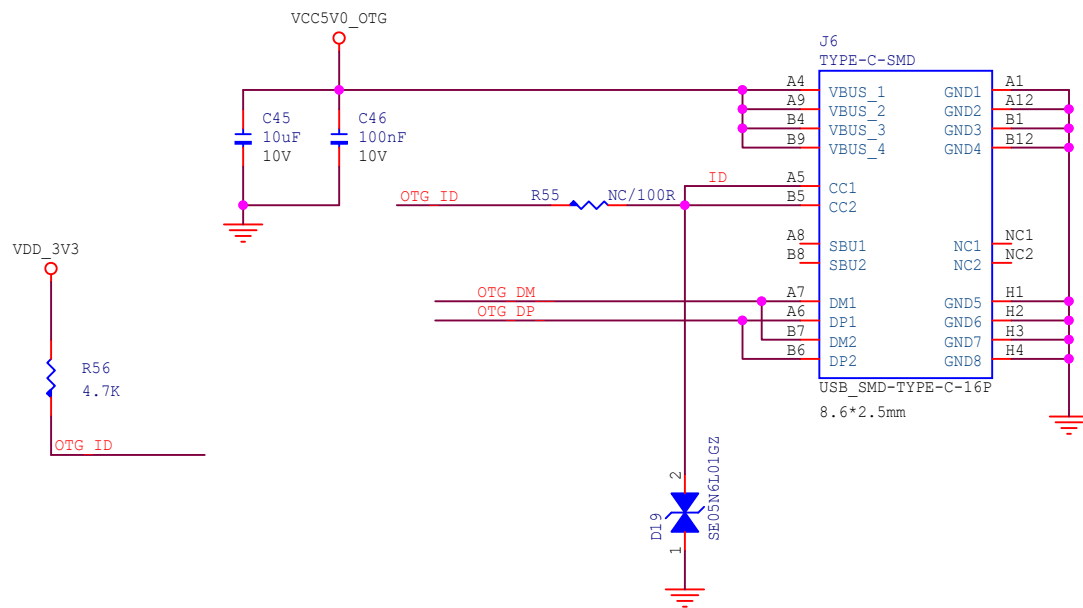
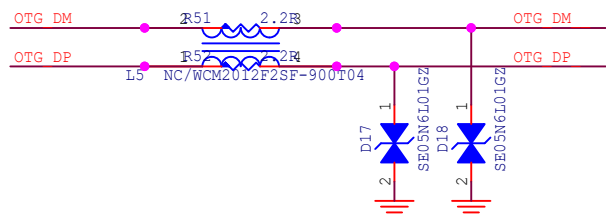
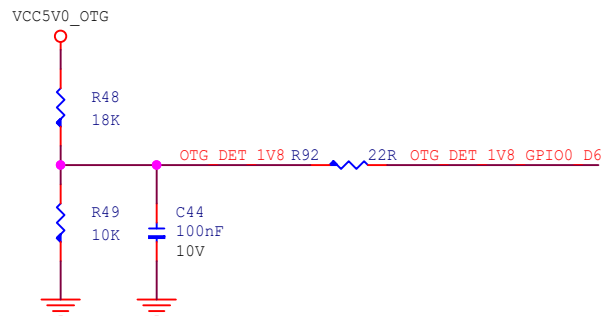
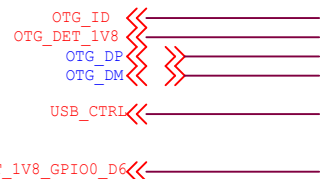
LED



RECOVERY



USB2.0 OTG



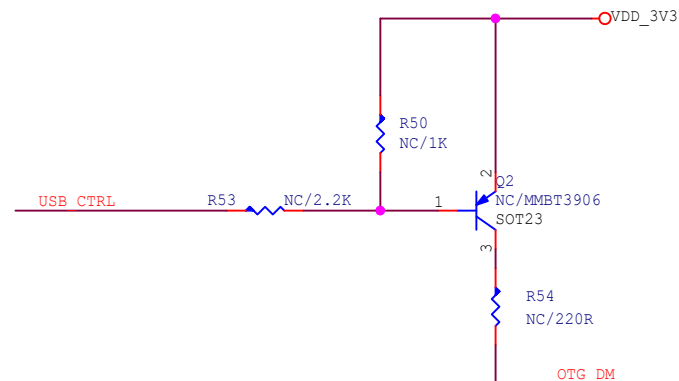
USB2.0 design rules:

1. Max intra-pair skew <4ps
2. Max trace length<6inchs
3. Max allowed via <6
4. Trace impedance 90ohm+/-10%
5. The distance between other signals follows the 3W rule.

This circuit is used to improve usb compatibility.

Note:

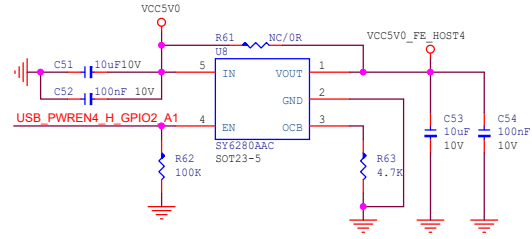
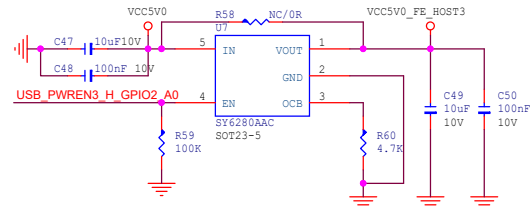
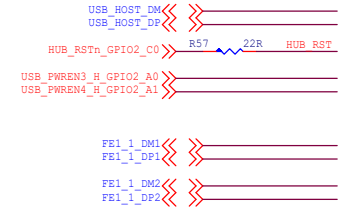
These components are close to R2502 to avoid long branches.



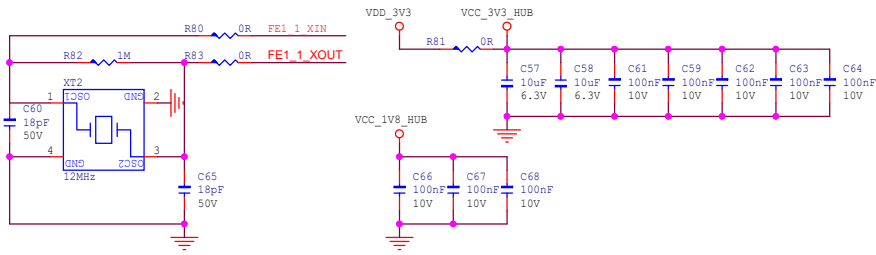
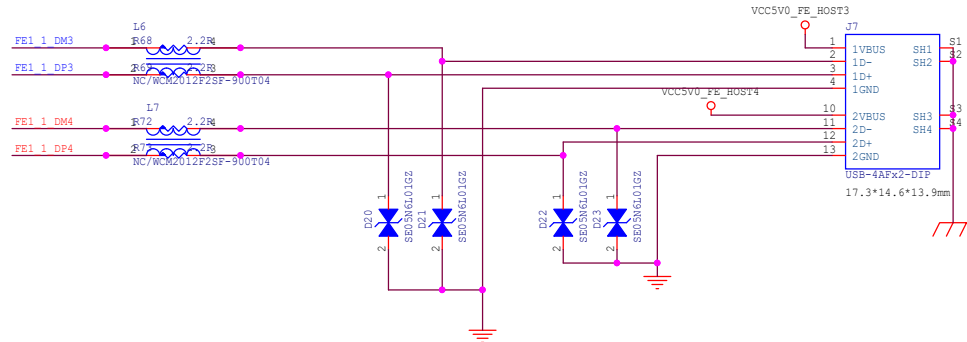
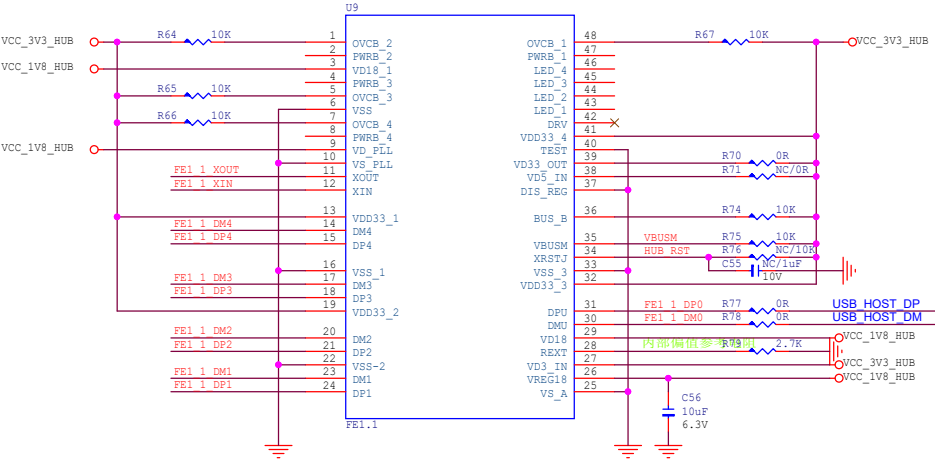
Rockchip Electronics Co., Ltd

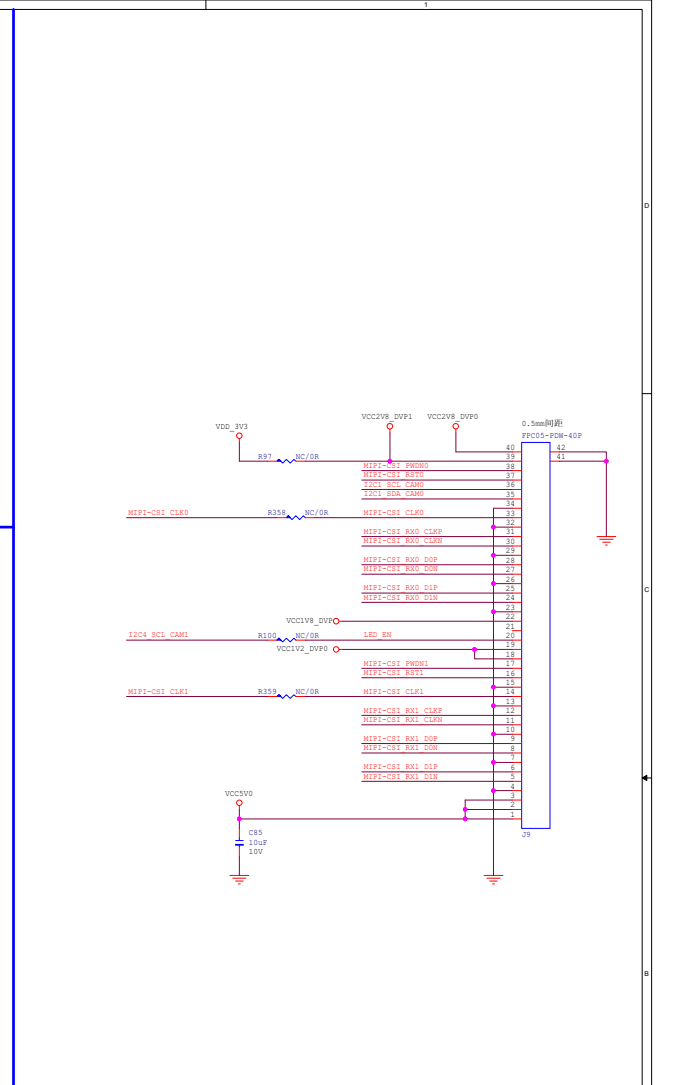
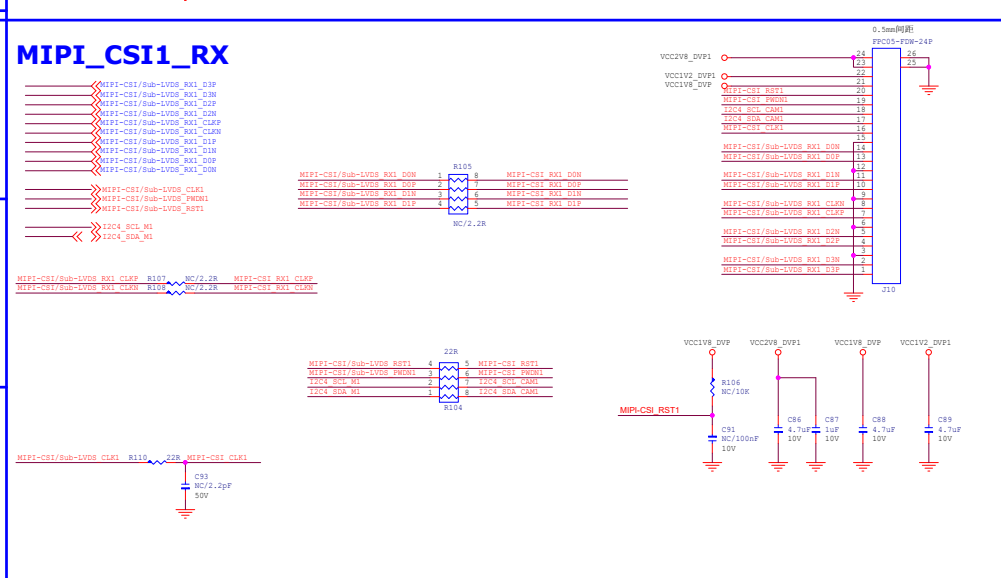
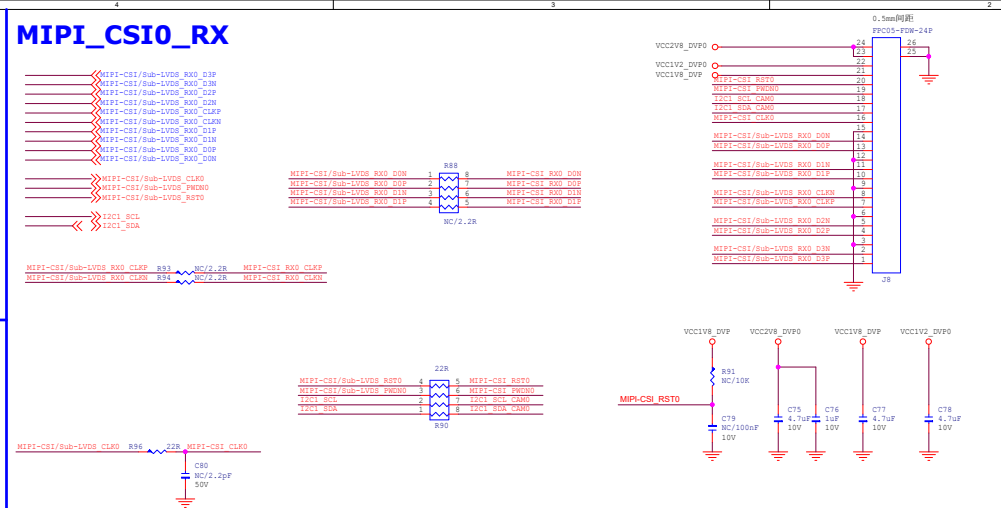
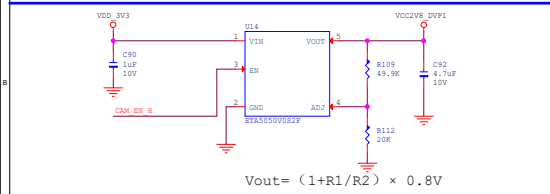
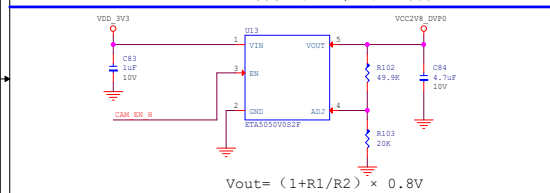
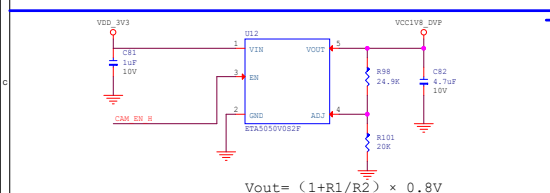
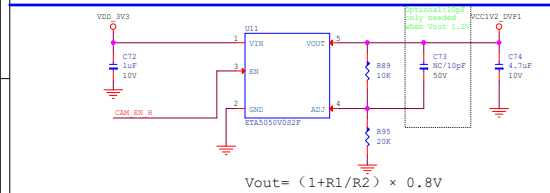
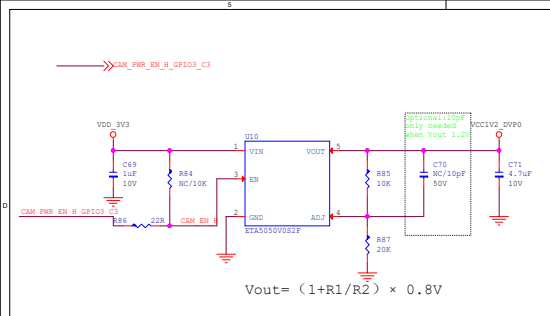
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	27.USB OTG				
Date:	Thursday, September 21, 2023			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	3 of 16

USB



USB2.0 HUB-FE1.1



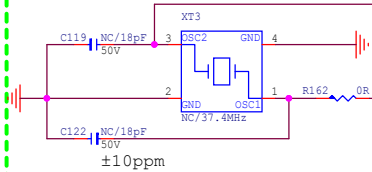


SDIO WIFI/BT MODULE

WIFI_WAKE_HOST_GPIO1_D1
WIFI_REG_ON_H_GPIO1_D0
BT_RST
BT_WAKE_GPIO1_A2
BT_WAKE_HOST_GPIO1_A3
PCM_SYNC
PCM_CLK
PCM_RX
PCM_TX
UART0_TX
UART0_RX
UART0_CTSN
UART0_RTSN
SDIO_D3
SDIO_D2
SDIO_D1
SDIO_D0
SDIO_CMD
SDIO_CLK
RK809_CLK_32K
WIFI_PWREN_H_GPIO3_C1



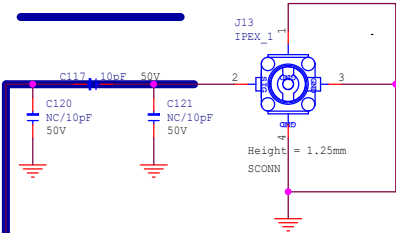
Note:
Adjusted the load capacitance
according to the crystal specification.



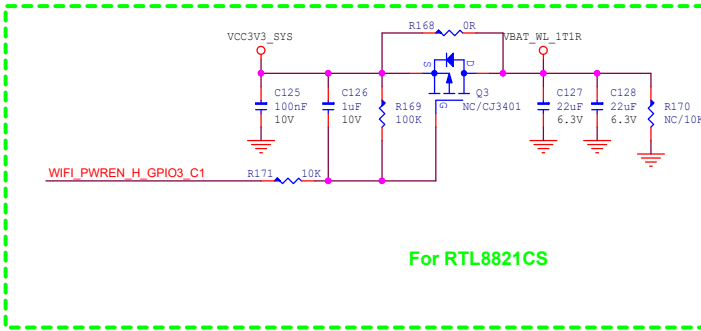
Option1

Using RTL8189ETV/FTV modules,
please notice
WIFI REG ON is on pin12 or pin34,
choose
according to the actual condition

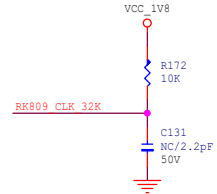
50 Ohm RF trace



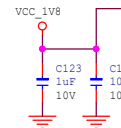
The maximum peak current is 600mA
Close to WIFI module



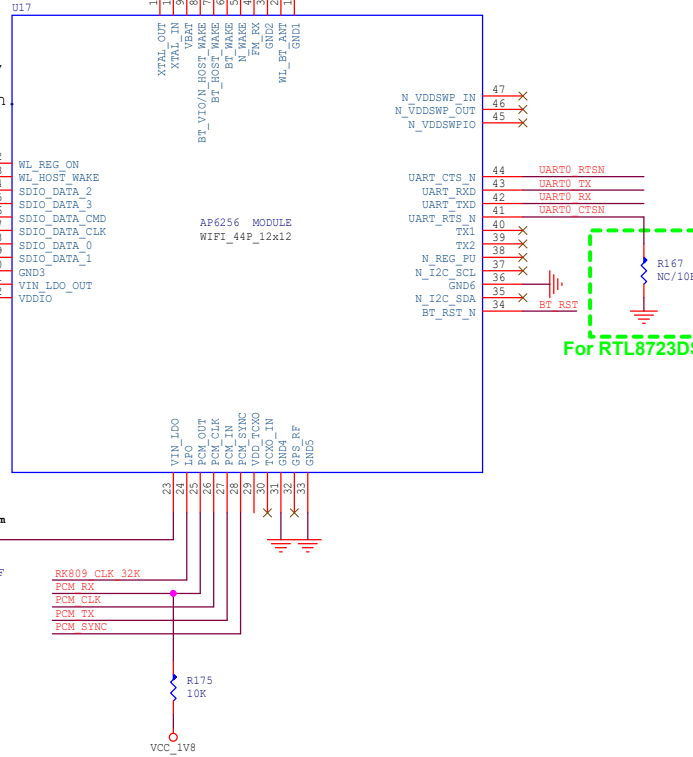
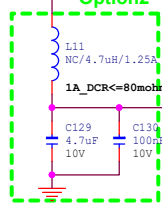
For RTL8821CS



WIFI_REG_ON_H_GPIO1_D0 12
WIFI_WAKE_HOST_GPIO1_D1 13
WIFITIR_D2 14
WIFITIR_D3 15
WIFITIR_CMD 16
WIFITIR_CLK 17
WIFITIR_D0 18
WIFITIR_D1 19
WIFITIR_D2 20
WIFITIR_D3 21
WIFITIR_CMD 22



Option2



Note:
Yes: option circuit be mounted
No: option circuit not be mounted

OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71~3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71~3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71~3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8~3.3V	No	No	No	No
RTL8723BS Module F23BDSM23-W2	No	Yes	No	No	4.0	Module Integrated	1.62~3.6V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62~3.6V	No	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7~3.45V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7~3.45V	No	No	No	No

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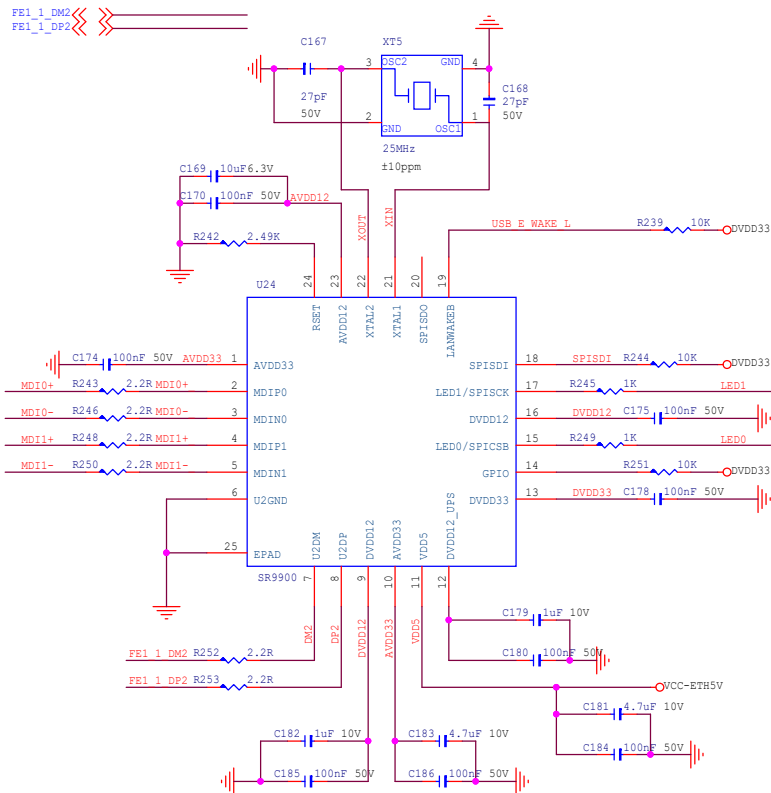


Diagram illustrating the RJ45 pinout for two ports, D71 and D72, connected to a network switch.

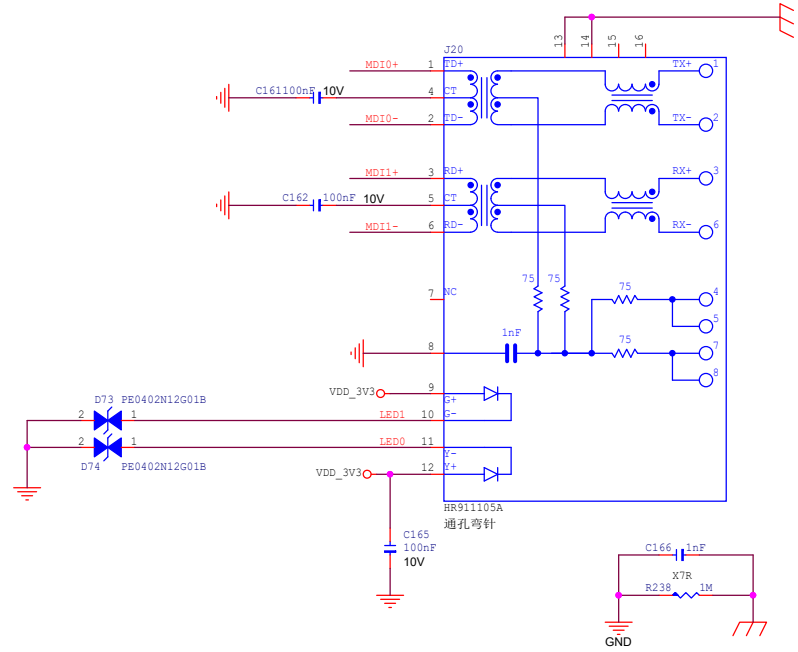
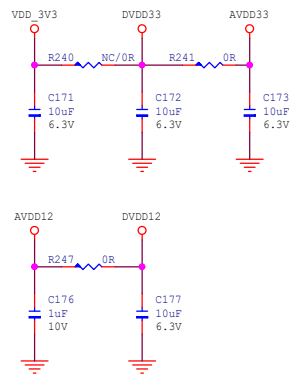
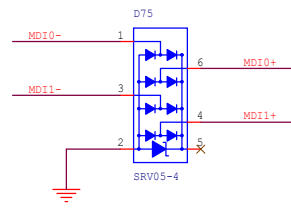
Port D71:

- Pin 1 (A): MDIO+
- Pin 2 (B): Unconnected
- Pin 3 (C): MDIO-
- Pin 4 (D): Unconnected

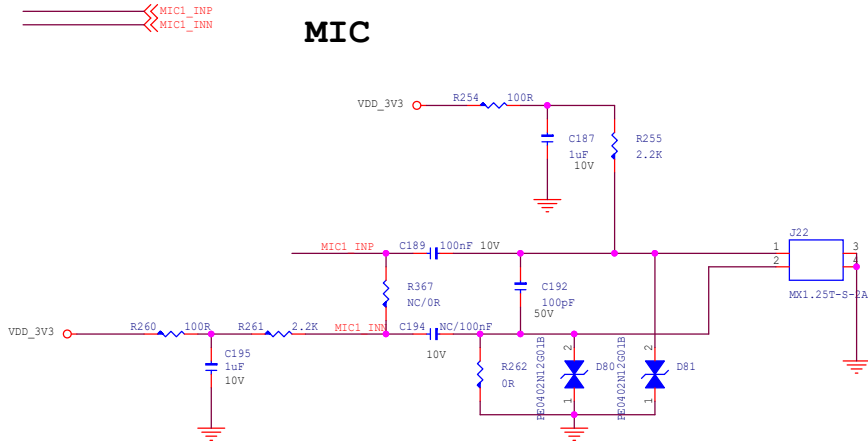
Port D72:

- Pin 1 (A): MDII+
- Pin 2 (B): Unconnected
- Pin 3 (C): MDII-
- Pin 4 (D): Unconnected

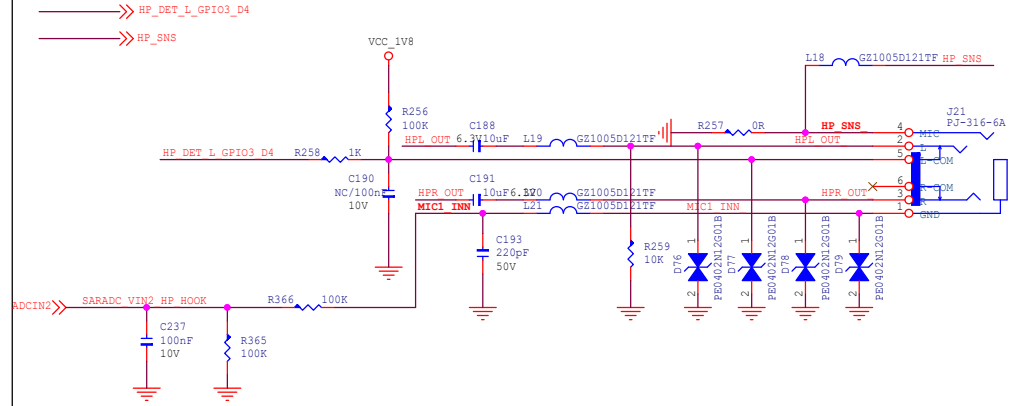
Both ports are labeled SE05D3L01GE.



MIC



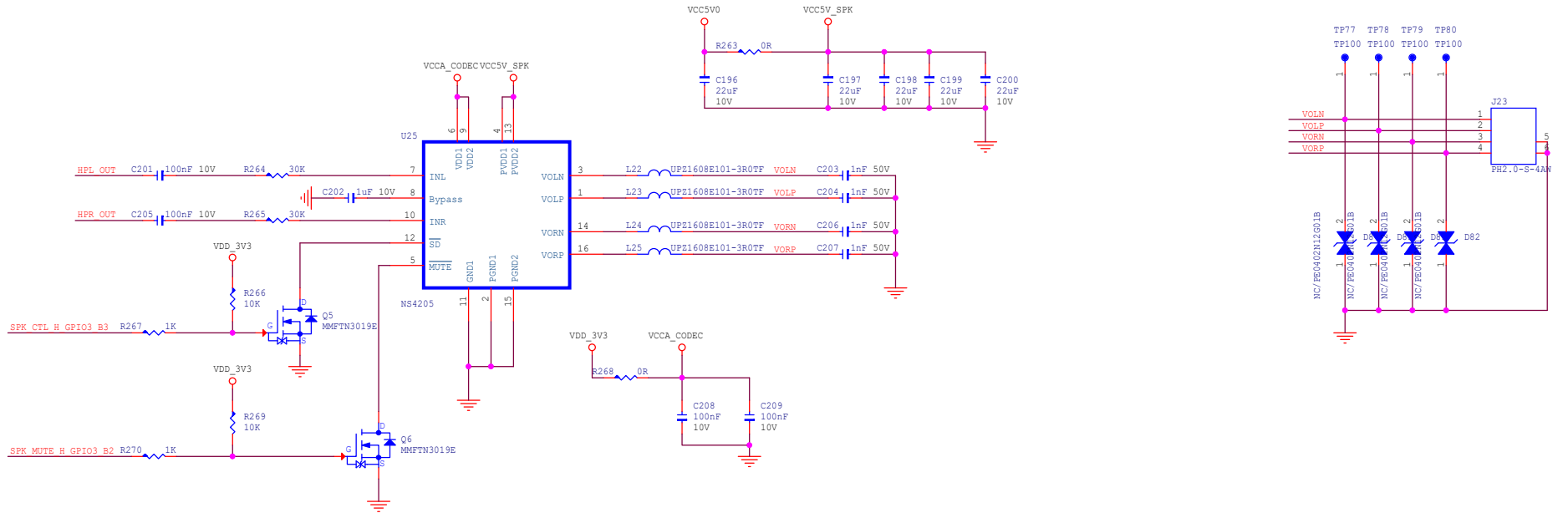
EPHONE



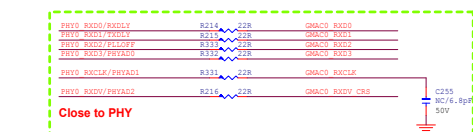
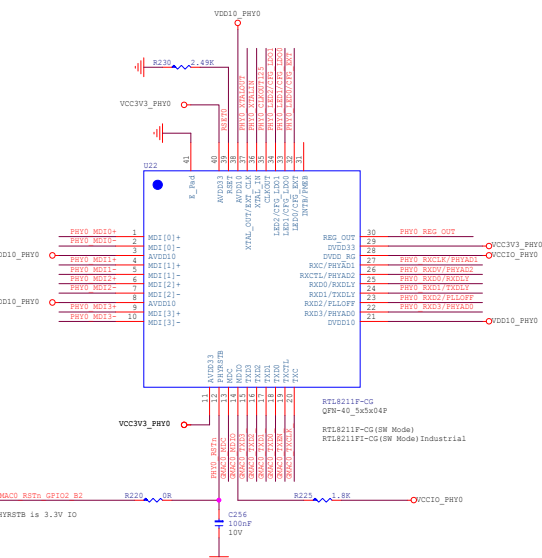
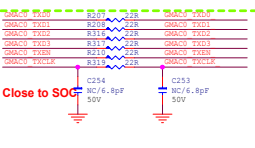
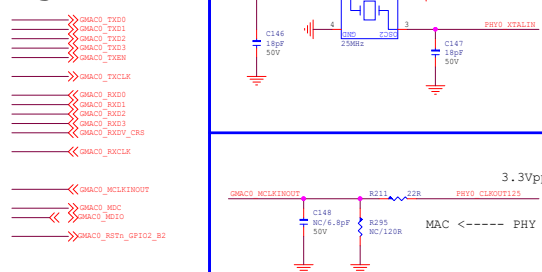
SPK

HPL_OUT
HPR_OUT

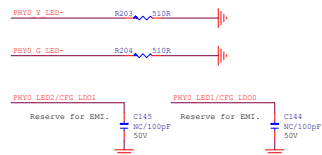
SPK_CTL_H_GPIO3_B3
SPK_MUTE_H_GPIO3_B2



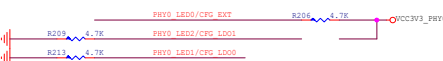
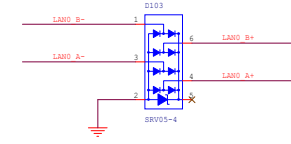
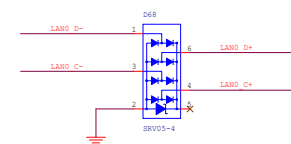
Giga PHY



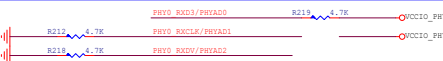
BOMIE Power Source	CFG_EXT	CFG_LDO1[10]
External 3.3V (default)	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V	1'b0	2'b10



PHY0_MD13-	R321	2.2k	LAND D-
PHY0_MD13+	R32	2.2k	LAND D+
PHY0_MD12-	R32	2.2k	LAND C-
PHY0_MD12+	R32	2.2k	LAND C+
PHY0_MD11-	R22	2.2k	LAND B-
PHY0_MD11+	R22	2.2k	LAND B+
PHY0_MD10-	R22	2.2k	LAND A-
PHY0_MD10+	R22	2.2k	LAND A+



VCC_PHY0_IO Voltage Config



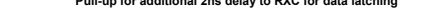
PHY Address Config



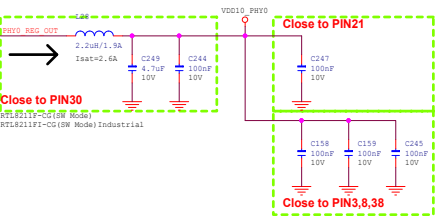
Pull-up for additional 2ns delay to RXC for data latching



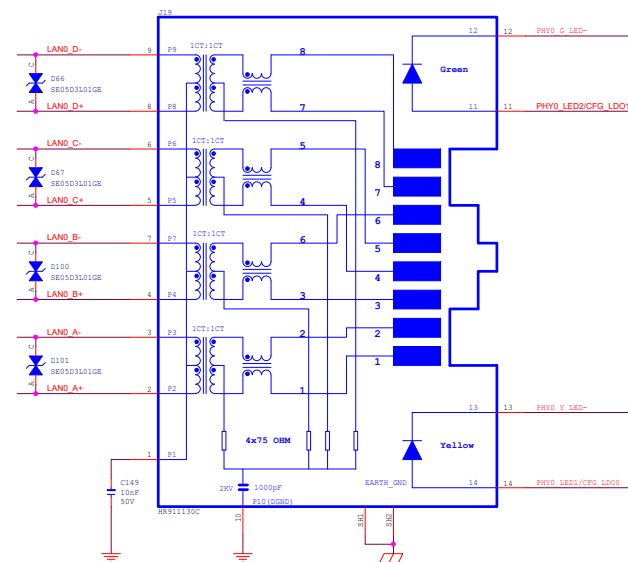
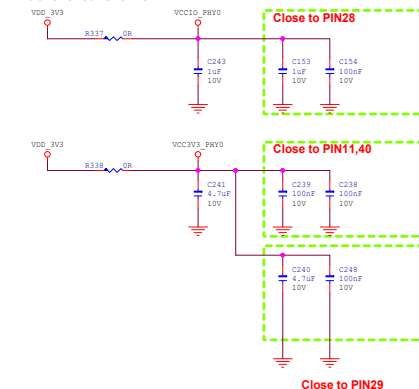
Pull-up for additional 2ns delay to TXC for data latching

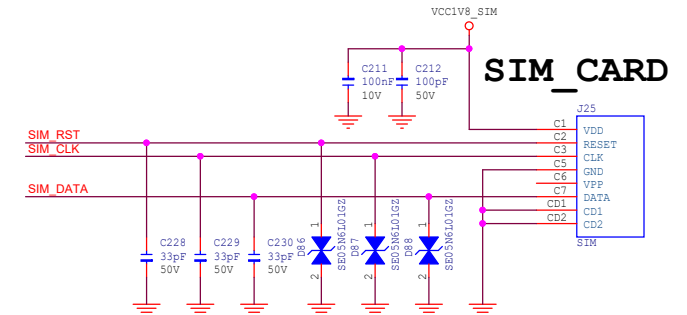
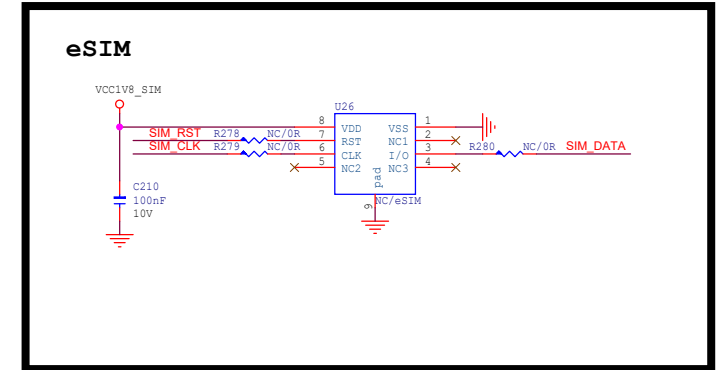
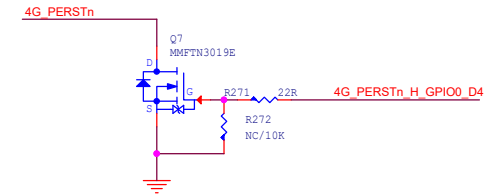
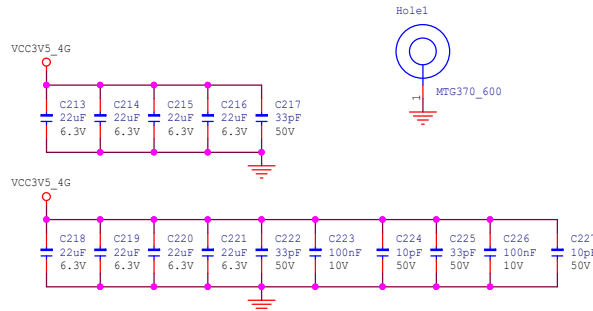
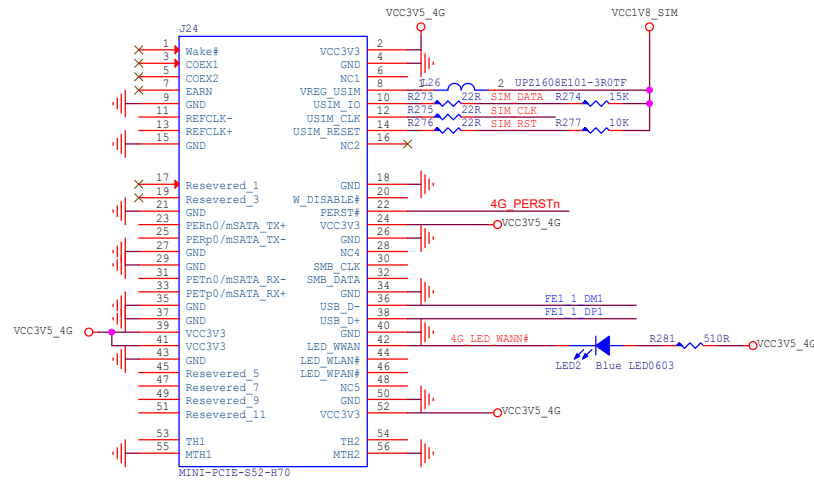
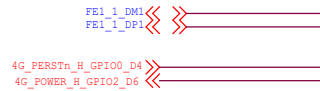


Pull-up to disable PLL @ ALDPS mode(Low power mode)

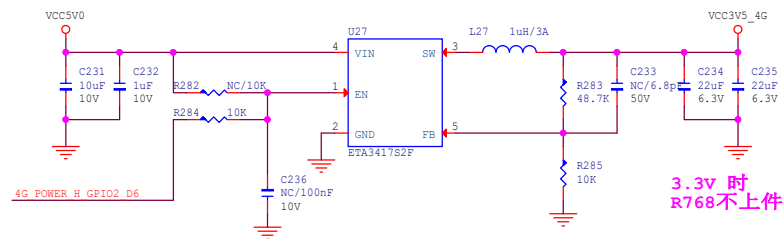


Note:
According to the actual
choice of mounted
Cannot be mounted
at the same time






4G/5G_POWER

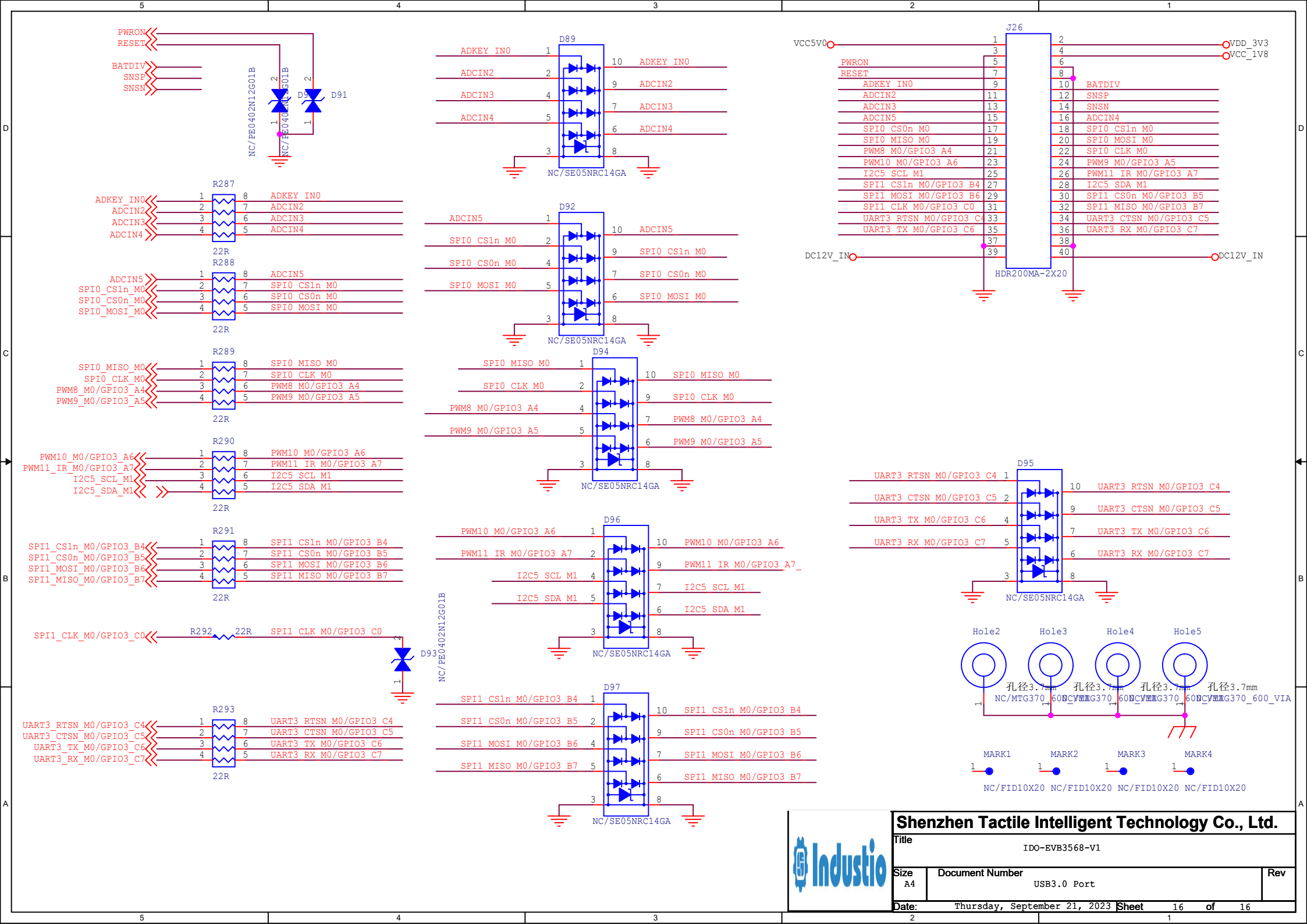



$$V_{out} = (1 + R1/R2) \times 0.6V$$

$$EN \geq 1.5V$$

3.3V 时
R768不上件

				Shenzhen Tactile Intelligent Technology Co., Ltd.			
				Title			
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